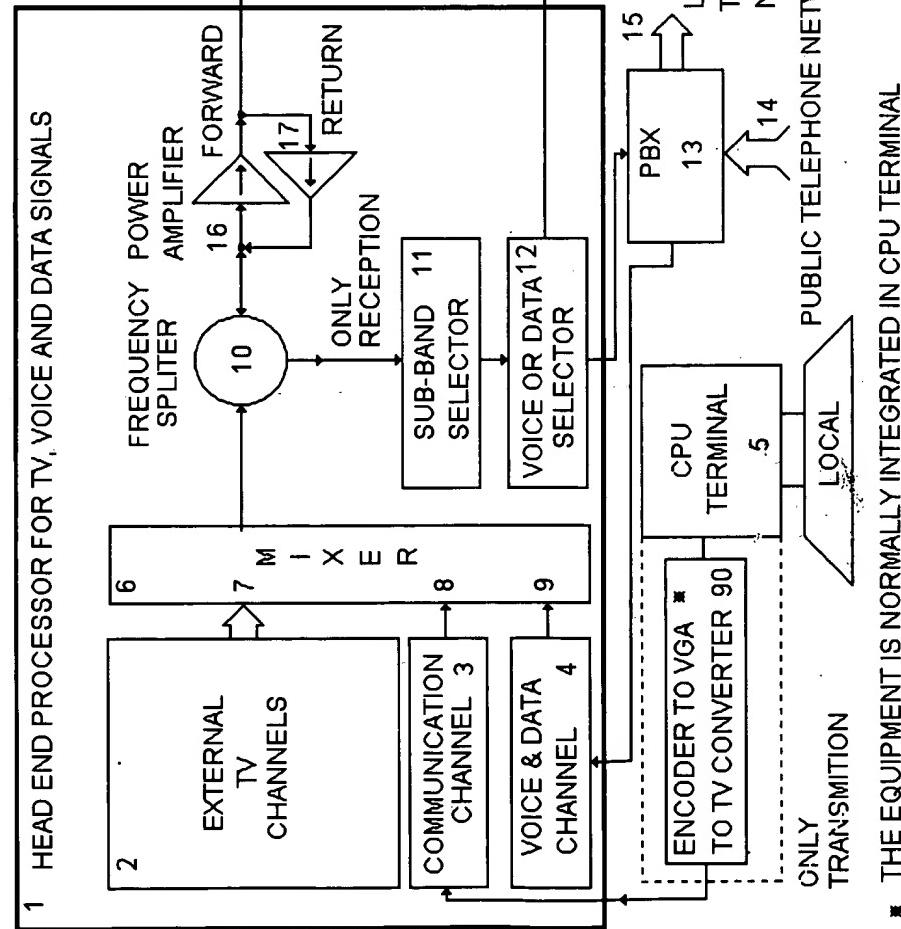




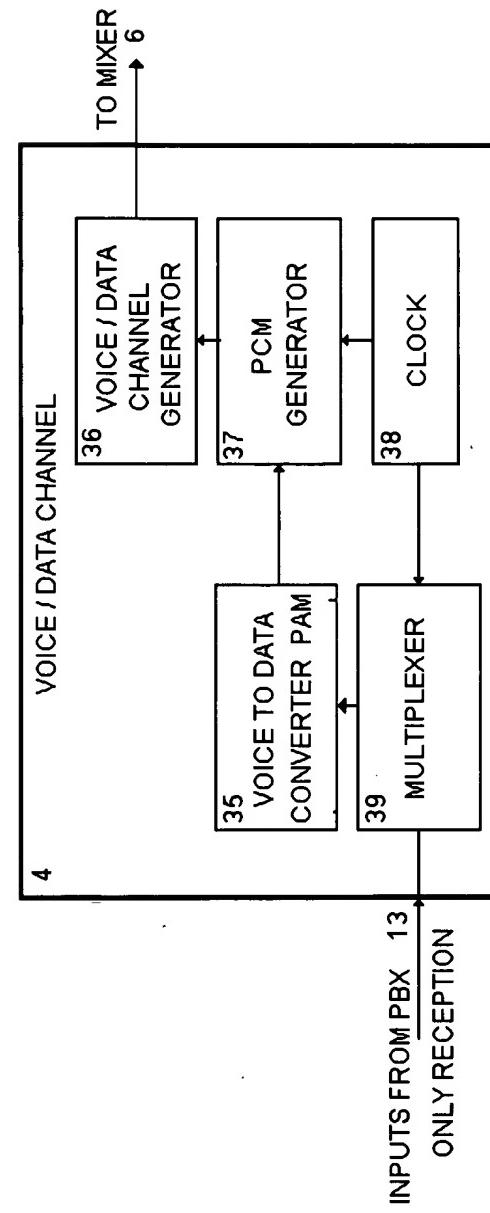
Fig. 01



THE EQUIPMENT IS NORMALLY INTEGRATED IN CPU TERMINAL



Fig. 02



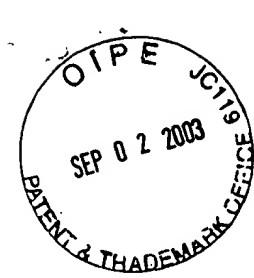


Fig: 03

INFORMATION FORMAT FOR EACH ONE OF THE 10 LINES IN FIRST PLACE

